High-Efficiency GaAs-based pHEMT Power Amplifier Technology for 1-18 GHz

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Abstract

Performance and reliability data for a high-efficiency microwave power amplifier design utilizing AlGaAs/InGaAs/GaAs pHEMTs are reported. A single stage MIC amplifier fabricated with a 5.6 mm gate width pHEMT resulted in P_{out}=2.5 W and PAE=73% at 4 GHz. Twenty three amplifiers with similar performance were built with devices from 4 different wafer lots. Currently, these amplifiers are undergoing an RF lifetest and have shown no change thus far to the 2000 h point. This GaAs-based pHEMT device technology supports amplifier module designs in the 1-18 GHz frequency range with output powers up to 20 W.

Introduction:

High efficiency power transistors are a critical building block of solid-state power amplifiers (SSPAs) for applications such as satellite communication systems. A multitude of these high-performance applications exist at the C-, Ku, and K-bands. Now emerging are additional high-performance, high-volume space applications at even lower frequencies (L- and S-Band) for new wide-area mobile communications systems. For these types of applications, the pseudomorphic HEMT (pHEMT) has shown the potential for high power, high efficiency performance (1-3). In this work, amplifier performance and reliability results obtained using a high breakdown voltage pHEMT device technology (4) are reported.

Device Structure and Fabrication:

The double-doped $Al_{0.24}Ga_{0.76}As$ / $In_{0.15}Ga_{0.85}As$ / GaAs pHEMT structure (Figure 1) is grown by molecular beam epitaxy (MBE). The double modulation doping scheme was implemented to achieve a sheet charge density of $n_s \approx 2.5 \times 10^{12}$ cm^{-2}. The measured room temperature Hall sheet charge density and mobility for this structure are 2.38 x 10^{12} cm^{-2} and 6,700 cm^2/V-s, respectively.

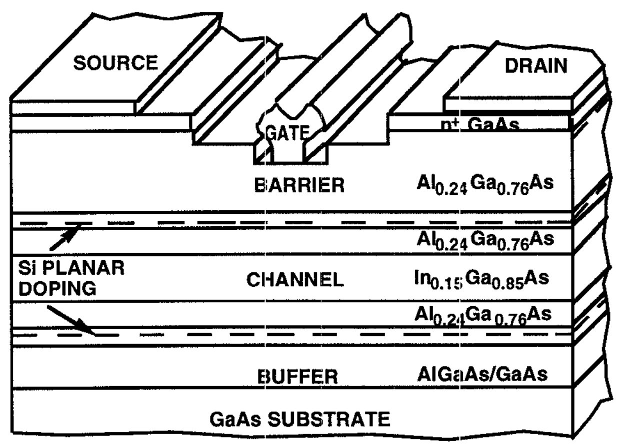

Figure 1: Cross-section of 1-18 GHz pHEMT device structure.

The device fabrication process begins with deposition of Ni/AuGe/Ag/Au source-drain ohmic contacts. A boron implant is then used to isolate the active region. Next, the ohmic contacts are alloyed at 420° C for 30 seconds in a forming gas ambient, resulting in a specific contact resistance of 0.25 ohm-mm. The gate recess was then performed with a two-step nonselective etch using a citric-acid based etchant (5). A source-drain spacing of 3 mm and channel recess width of 1.5 mm were found to result in the best combined dc and RF performance. The 0.25 mm gates were formed by e-beam lithography and deposition of Ti/Pt/Au metalization. Finally, a 1000Å layer of silicon

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nitride was deposited for device passivation and air-bridge interconnect metal was fabricated. The wafer was thinned to 50 mm to reduce the thermal resistance and backside vias were formed to provide contact to the sources.

Device and Amplifier Performance:

Devices were fabricated with total gate periphery of 0.4 mm to 19.6 mm. Figure 2 shows the I-V characteristics of a 0.25 µm x 0.4 mm wide pHEMT. The dc performance is characterized by a maximum transconductance of 280mS/mm, I_{max}=490mA/mm (at V_{gs}=+1.0 V), and gate-drain breakdown voltage (source floating) of $|BVgd|$=21.5 V measured at $|I_{gd}|$=1 mA/mm (see inset to Fig. 2). Devices from 4 different wafer lots produced similar results. The dc parameters scaled well to the largest devices (19.6 mm gate periphery). For all wafer lots, $|BV_{gd}|$ for passivated devices was consistently in excess of 18 V, with some samples as high as 25 V. The repeatability and scaling of breakdown voltage is a critical device parameter for reliability and performance.

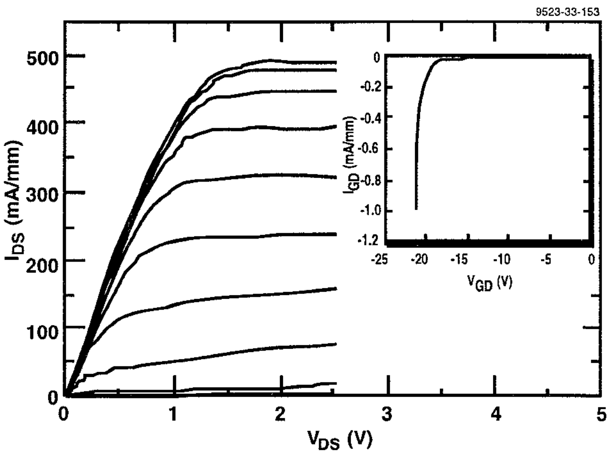
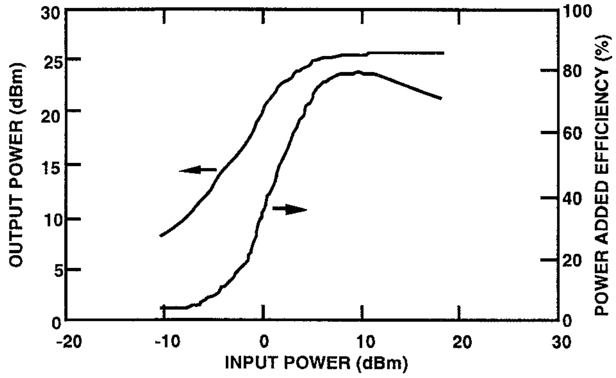
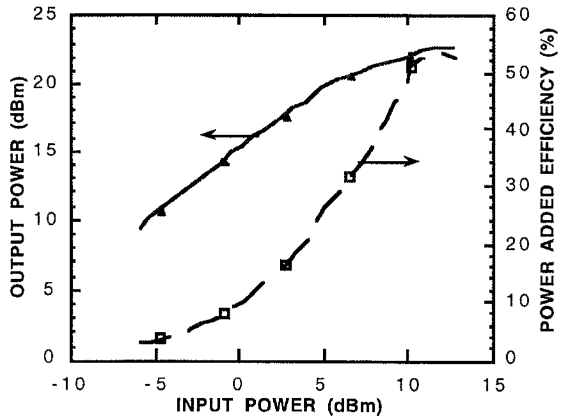


Figure 2: IV characteristic for a 0.25 µm x 400 µm pHEMT device and the gate-drain breakdown voltage curve. Here V_{gs} is varied from +1.0 V to -1.25V in steps of -0.25 V.

On-wafer power measurements were performed on 1.2 mm and 0.448 mm gate periphery devices using an active load-pull CW measurement system (6) at 4.5 GHz and 18 GHz, respectively. A plot of the on-wafer measured output power (P_{out}) and PAE at 4.5 GHz and V_{ds}=5 V is shown in Figure 3a. A maximum PAE of 79% is obtained at P_{out}=25.4 dBm (0.35 W, 0.29 W/mm). PAE was improved 8-10% by tuning the second harmonic (9 GHz) and 2-3% with third harmonic (13.5 GHz) tuning. The data obtained with this measurement system assumes a conjugate input match for the device.



(a)

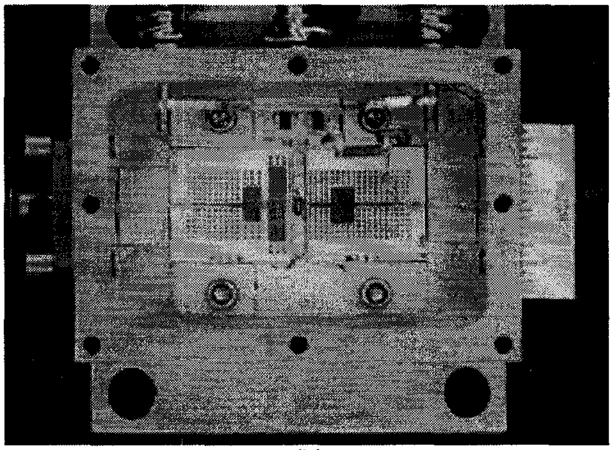


(b)

Figure 3: On-wafer active load pull measurement of (a) 0.25 µm x 1200 µm pHEMT device demonstrating maximum PAE = 79% and P_{out} = 0.35 W at 4.5 GHz and of (b) 0.25 µm x 448 µm pHEMT device demonstrating maximum PAE = 54% and P_{out} = 0.18 W at 18 GHz.

Increasing V_{ds} to 7 V resulted in a significant increase of output power with a small decrease in PAE. With V_{ds}=7 V, the measured data were PAE= 76%, P_{out}=28.1 dBm (0.65 W, 0.54 W/mm). A plot of the on-wafer measured output power and PAE at 18 GHz and V_{ds}=3 V is shown in Figure 3b. Here, a maximum PAE of 54% was obtained at an output power of 22.6 dBm (0.18 W, 0.4 W/mm). Our findings show that a high voltage, low current fundamental load line is necessary for high PAE operation.

The load impedances measured for the 1.2 mm wide pHEMT were scaled to estimate the optimum load impedances for a single-stage power amplifier with a 5.6 mm wide device. A photograph of the 5.6 mm pHEMT amplifier is shown in Figure 4.



(b)
Figure 4: Photograph of the 4 GHz, 5.6 mm gate periphery pHEMT amplifier.

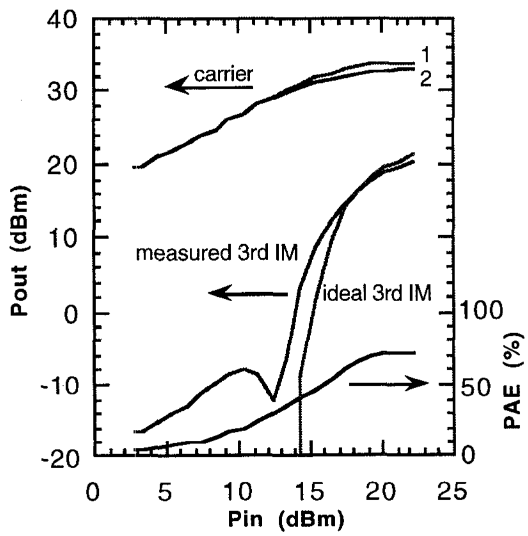


Figure 5: Measured power added efficiency and output power of the 5.6 mm gate periphery pHEMT amplifier.

The fundamental and harmonic load impedances presented to the device for best performance scale fairly well from the on-wafer results. The amplifier input was conjugately matched, and a 2nd harmonic input termination was added which produced a ≈6-8% efficiency increase. All efforts were made to minimize losses in the RF and dc circuitry. Resistive damping circuitry was used to make the amplifier critically stable in-band (K=1, B1>0). Inductors were used for bias on both the input and the output. On the input, the inductor allowed easy adjustment of the amount of damping. On the output, an inductor was used so that harmonic terminations set by the MIC circuitry would not be affected. The measured output power at V_{ds}=7 V was 34 dBm (2.5 W, 0.4 W/mm) with PAE=73% and operating gain of 13.5 dB at 3 dB gain compression. A two-tone linearity measurement was made on the amplifier (carrier spacing=2 MHz). The linearity performance of the amplifier is characterized by a C/3IM curve which approaches that of an ideal limiter (see Figure 5).

Twenty three pHEMT amplifiers were assembled and measured with devices from 4 different wafer lots. Similar performance to that reported above was obtained for each of these amplifiers, with P_{out}=2-2.5 W and PAE=67-74%, as seen in Figure(s) 6 (and 7).

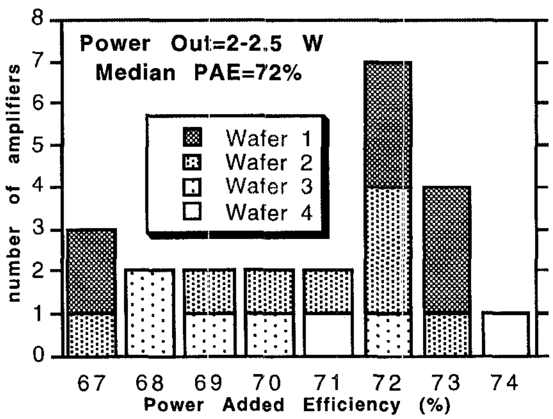


Figure 6: Histogram of PAE for fabricated amplifiers with devices from 4 different wafer lots (each wafer lot designated by a different shade).

All MIC circuitry was printed, with no tuning done on the output substrate. On the input, slight adjustments had to be made to the first pole of the matching circuitry to account for variability of C_{gs} from wafer to wafer. To demonstrate low frequency performance of the pHEMT device technology, an amplifier module was built with two 19.6 mm wide parts. The measured performance at 1.5 GHz and V_{ds} = 7 V was P_{out}=14 W with PAE = 68%. All of the quoted amplifier results were made in a system calibrated from coaxial connector to connector with V_{ds} measured external to the circuit.

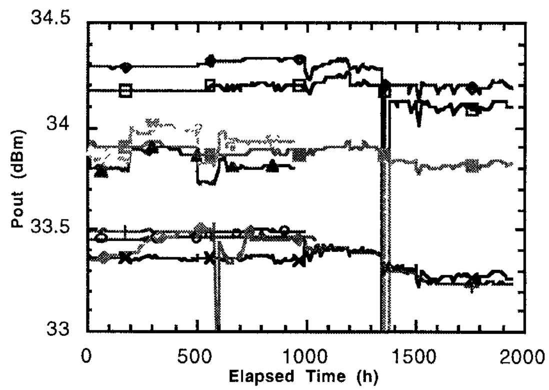


Figure 7: RF lifetest trend data for 11 amplifiers.

Reliability:

PHEMT devices and amplifiers are undergoing dc and RF lifetests. For the dc lifetest, 1.0 mm gate periphery devices are being stressed at baseplate temperatures of 160°, 180°, and 200° C. DC reliability results will be presented.

An automated RF system has been constructed for the amplifier lifetest. All dc currents, voltages, and RF power levels are monitored. Eleven of the 2 W amplifiers were put on lifetest and have now accumulated ≈2000 h. The amplifiers are being operated at V_{ds}=7 V and ≈3 dB gain compression. Figure 7 shows the trend data for P_{out} of the amplifiers. The devices show an initial $V_{pinchoff}$ shift that produces an ≈-10% $I_{ds,no\ drive}$ change in the first ≈48 h and then are seen to stabilize. This shift does not affect P_{out}, as it remains unchanged (i.e. no power slump has been observed to within measurement error).

An RF step stress test (steps in drain voltage and RF drive) is planned for these devices/amplifiers. These results will determine maximum safe voltage and current limits for the pHEMT devices when operated in the high-voltage load line circuits that produce these high efficiency results.

Conclusions:

A high breakdown voltage GaAs-based pHEMT device technology for the 1-18 GHz frequency range has been reported. Twenty three fabricated power amplifiers obtained P_{out}=2-2.5 W with PAE of 67-74% at 4 GHz. DC and RF lifetests are ongoing with these devices and results to date indicate that this device process and amplifier design should prove reliable for space applications. Currently, amplifiers with one and two devices of total gate peripheries up to 25 mm each are being fabricated. Module output powers of up to 20 W with efficiencies approaching 70% are predicted based on the performance reported here.

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